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REMARKS

Examiner Berezny is thanked for his examination of the subject Patent Application. The Specification and Claims have been carefully reviewed with respect to the cited prior art, the Claims are considered to be in condition for Allowance.

DETAILED ACTION

Action Items 1, 2 & 9

Claim Rejections - 35 USC § 112

The Examiner writes:

> 2. Claims 8 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The use of "and" in the claim requires that all the listed materials appear in the low-k dielectric. The specifications appear not to teach this combination of materials, see p .19.
>
> 9. Applicant's arguments filed 2/10/03 have been fully considered but they are not persuasive. Applicant asserts that claims 8 and 25 have been amended to overcome their rejection under 35 USC 112, par.2. Such an assertion is incorrect. Claims 8 and 25 have not been amended and the rejection stands.

The Applicants had previously amended Claims 8 & 25 but neglected to move them together with Claims 10 & 28 from the draft copy to the submission copy. They now appear herein, as marked up and in the clean copy.

Action Items 3, 4, 10, 11 & 12

35 USC § 102 Claims Rejection

Reconsideration of the rejection of Claims 1, 3-5, 7-10, 12-16, 18-20, 22, 25-26, 28 and 30 under 35 USC §102(e) as being anticipated by Zhou et al (6,358,842) is requested based on the following arguments:

The Examiner again presents the rejection argument as follows:

4. Zhou teach s a method to solv via poisoning for insulative porous low-k materials, see abstract, comprising the steps of: providing a silicon substrate, col.3, ln. 55-57, having a silicon nitride passivation layer with a thickness of 30-1000 Angstroms, col.4, ln.12-15, formed over a first metal layer formed on said substrate; fig.4, el.50, 58, and 54, forming a first insulative layer, with a thickness of 2000-100000 Angstroms, col.4, ln.49-52, over said substrate; el.62, forming a silicon nitride etch-stop layer, col.4, ln.60-63, with a thickness of 30-1000 Angstroms, col.4, ln.65-67, over said first insulative layer; el.66, forming a second insulative layer, with a thickness of 2000 to 100000 Angstroms, col.5, ln.34-37, over said etch-stop layer; el.70, forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern; fig.5, el.78, etching said first and second insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer; fig.5, removing said first photoresist mask; *forming a low-k protection layer over said substrate, including in said hole opening; fig.6, el.82*, forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern; fig.9, etching said second insulative layer through said trench pattern in said second photoresist mask to form a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate; fig.1 0, *removing said second photoresist mask; fig.11, removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;* fig.6, el.82, removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer; fig.7, el. 82, 86, forming a barrier layer over said substrate, including in said dual damascene structure; fig.13, el.1 04, depositing a second metal, such as copper, over said barrier layer in said dual damascene structure; fig.13, el.106, and performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure, col.8, ln.6-63. **Further, Zhou teaches forming a low-k protection layer comprises Si02, SiN, SiC and SiNCG, col.6, ln.18-25, wherein said low-k protection layer has a thickness between about 20 to 1000 Å,. col.6, ln.46-50,** and wherein said barrier layer comprises Ta,. Ti, TaN, TiSIN, TaSiN,. WN, col.8, ln. 58-58.

Agreement

The Applicants agree with the Examiner that the underlined passages represent a prior art description of a semiconductor damascene process. The passages in italics represent areas in which Zhou et al. have made their inventive contribution but the account is not accurate.

Disagreement # 1

The Applicants again disagree. The passage in bold print is in error. The low-k

protection layer compounds **SI02, SiN, SiC and SiNC** are **not** found discussed anywhere in the specification of Zhou et al. let alone in column 6, lines 18-25. Zhou et al. provides a sulfur based low-k protection layer thickness of 5 - 100Å

Column 6, lines 18 - 25 read:

> As a unique feature of the present invention, a sulfur-containing gas is used in place of the oxygen plasma to strip away the photoresist layer 78 and the optional organic BARC layer. This sulfur-containing gas reacts with the first and second low dielectric constant layers 62 and 70. The reaction of the sulfur-containing gas with the organic or carbon-doped materials results in a sulfating or sulfonating action. The result of the reaction is the formation of a sulfur-containing sidewall passivation layer 82 on the sidewalls of the low dielectric constant layers 62 and 70.

In the response to the Applicants' previous arguments the Examiner writes:

> 10. On p.9 of applicant's response, applicant asserts that Zhou fails to teach the formation of SiO2 in forming a protection layer. Applicant's attention is directed to col.8, ln.5-20, which further elaborates on the reaction chemistry. Note that the sulfur containing gases consist of SO2 and SO3 and further include oxygen gas. During the sulfating and. sulfonating reactions the oxygen will react with the silicon and thus form SiO2 at claimed. The sulfur-containing layer also contains silicon dioxide.

The Applicants do focus their attention on column 8, lines 5-20 of Zhou and read:

> The sulfur-containing gas comprises sulfur dioxide (SO.sub.2), sulfur trioxide (SO.sub.3), or a mixture of sulfur dioxide and sulfur trioxide. The second sidewall passivation layer 98 formed by the sulfating or sulfonating reaction has a thickness of between about 5 Angstroms and 100 Angstroms. The present invention forms the second sidewall passivation layer 98 at a relatively low temperature. The novel approach of the present invention forms the advantageous second sidewall passivation layer 98 without any additional processing steps.
>
> As a further alternative, oxygen gas may be added to the sulfur-containing gas in the same reaction chamber conditions, with or without plasma generation. In this case, the ratio of the flow rate of oxygen to the flow rate of the sulfur-containing gas is between about 1:1000 and 1:1.

Yet the Applicants cannot see any reference to "SiO_2" (Silicon dioxide) or SiN, SiC or SiNC in the formation of a protective layer in these passages. They observe only "SO_2" (Sulfur dioxide). Sulfur dioxide is not Silicon dioxide. There is

NO teaching of formation of "SiO_2". A thorough review of Zhou et al. only shows that "SiO_2" may be a component of an applied low-K dielectric layer but not a component of a protective layer.

Column 4, line 24-46 as an example read:

> The first low dielectric constant layer 62 preferably comprises organic material, carbon-doped silicon dioxide, or hydrogen-doped silicon dioxide. Alternatively, undoped silicon dioxide or fluorinated silicon dioxide may be used. Material types that fall under these descriptions and that could be used to form the first low dielectric constant layer 62 include, but are not limited to: porous organic materials, non-porous organic materials, porous fluorinated organic materials, non-porous fluorinated organic materials, porous hydrogen-doped silicon dioxide, non-porous hydrogen-doped silicon dioxide, porous carbon-doped silicon dioxide, and non-porous carbon-doped silicon dioxide. Specific materials include, but are not limited to: poly(arlene) ether or SILK.TM. by Dow Chemical Corp., fluorinated arylether or FLARE.TM. by Allied Signal Corp. or Honeywell Corp., amorphous fluorocarbon (.alpha.-C:F), polytetrafluoroethylene (PTFE.TM.) or Teflon.TM. by Dupont Corp., parylene-F, parylene, alkyl silsesquioxane, aryl silsesquioxane, poly(silazane), poly(arylene)ether, silica doped with methane or Black Diamond.TM. by Applied Materials Corp., carbon doped silicon dioxide or Coral.TM. by Novellus Corp., fluorinated poly(arylene) ether, and hydrogen silsesquioxane.

These are the low-K dielectric layers applied. They are not produced as the result of sulfonating during a photoresist removal step. Furthermore, with the variety of the above materials, if it were true, it would be incumbent upon Zhou to teach how each and every one of them produces a silicon dioxide or SiN, SiC or SiNC protective lining during a sulfonating process especially with photoresist but it is noticeably absent. Furthermore, there appears to be no silicon present for a reaction to form "SiO_2".

The Applicants assert that the instant invention is not anticipated by Zhou et al.

Disagreement # 2

Secondly, the italicized passages do not describe the instant invention. At

th point in the damascene process when the first etching is complete, Zhou et al. strip the photoresist using a sulfur base compound and in doing so simultaneously deposit a sulfur-containing layer on the sidewall of the via. Further into the damascene process when the second etching is complete, Zhou et al. again strip the photoresist using a sulfur base compound and in doing so simultaneously deposit a second sulfur-containing layer on all the exposed low-k dielectric surfaces. This double sulfur containing layer forms their low-K protection layer, perhaps twice on the previously deposited surface. Subsequently, a barrier layer of Ta, TaN, TiN, or WN is deposited as conventionally used for damascene copper deposition.

By contrast, but within the same or similar context, the Applicants provide a low-K protective lining to prevent poisoning the copper inlay. When stripping of the first photoresist is required, the Applicants do **not** make use of a simultaneous operation, but do require two separate operations which they can control separately. First, they use oxygen plasma etching to assure complete stripping of the photoresist. Then they deposit a single thin (50 to 400 Angstrom) film of **Si02, SiN, SiC or SiNC** on the sidewalls of the via by a blanket deposition over the second dielectric layer. Although there is a subsequent second photoresist operation for the trench without applying a protective layer, there was only one protective layer deposited and that was in the hole. A barrier layer of (note a larger family than that of Zhou et al.) Ta, Ti, TaN, TiSIN, TaSiN, or WN is then deposited.

Although th bulk of the description of both Zhou et al. and the instant

application is in the context of prior art damascene processes both Zhou et al. and the instant application disclose completely different m thods of precluding poisoning of copper deposited in low-K dielectric trenches and via holes. While Zhou et al. uses a simultaneous strip and deposit, the instant invention uses separately controlled operations. While Zhou et al. provides two protective coatings, the instant invention provides just one. While Zhou et al. deposit a sulfur containing layer, the instant invention deposits a silicon containing layer.

The Examiner writes in response to previous arguments:

> 11. Applicant argues that Zhou performs applicant's two steps simultaneously, but applicant's claims fail to require separate steps. A simultaneous step is within the scope of the claims.
>
> 12. Applicant also argues that Zhou teaches two protective coatings, while applicant teaches just one. The claims use the term "comprising", which broadens the scope of the claims to include extra steps and layers. . Action Items 5, 6 7 & 8

It should be noted that Zhou et al., in a claim 1 limitation, state:

> Simultaneously stripping away said first photoresist layer and forming a first sidewall passivation layer on the sidewalls of said via openings by using a sulfur-containing gas;

The Applicants respond by amending Claim 13 to clearly indicate two steps, one of removing the photoresist followed by the other of forming a protective layer on the same surface. To now attempt to read them in reverse order or simultaneously would not make sense.

Claim 1

> 1. (CURRENTLY AMENDED) A method to solve via poisoning for insulative porous low-k materials comprising the steps of:
>
> providing a substrate having a first and a second insulative layers separated from each other by an intervening etch-stop layer formed therein said substrate;
>
> forming a hole opening in said first and second insulative layers, including said

intervening tch-stop layer;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a trench opening over said hole opening to form a dual damascene structure;

forming a barrier layer on the vertical walls of said trench opening and on said low-k protection layer on the vertical walls of said hole opening;

forming a metal layer over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP), to complete the forming of said dual damascene structure.

Claim 13

13. (CURRENTLY AMENDED) A method to solve via poisoning for insulative porous low-k materials in a dual damascene structure comprising the steps of:

providing a substrate having a passivation layer formed over a first metal layer formed on said substrate;

forming a first insulative layer over said substrate;

forming an etch-stop layer over said first insulative layer;

forming a second insulative layer over said etch-stop layer;

forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern;

etching said first and second insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer;

removing said first photoresist mask from said second insulative layer;

forming a low-k protection layer over said substrate on said second insulative layer, including in said hole opening;

forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern; .

etching said second insulative layer through said trench pattern in said second photoresist mask to form a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate;

removing said second photoresist mask;

removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;

removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer;

forming a barrier layer over said substrate, including in said dual damascene structure, wherein said barrier layer conforms to said low-k protective layer in said hole opening and conforms to said trench in said second insulative layer;

depositing a second metal over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure.

Action Items 5, 6, 7, 13 & 14

35 USC § 103(a) Claims Rejection

Reconsideration of the rejection of Claims 11, 23-24, 27, and 29 under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. as applied to claims 1, 3-5, 7-10, 12-16, 18-20, 22, 25-26, 28 and 30 above, and further in view of Lin (US 6,140,220) is requested based on the following arguments:

The Examiner suggests the following:

6. Zhou appears, not to specify the thickness of the barrier film, nor the etch chemistry used to etch the first and second insulators, the etch stop layer, and the protective layer. Lin teaches forming a barrier layer comprising Ta or TaN, having a thickness of 100-2000 Angstroms, col.4, ln.18-23. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Lin with Zhou to use a barrier layer of the same material with a thickness used by Lin to prevent via poisoning, thereby reducing contamination of the interconnect structure.

The Applicants reply by noting that the objects of Lin are:

A further object on the invention has been that said dual damascene structure provide low via hole resistance between wiring levels without sacrificing the effectiveness of the diffusion barrier.

These objects have been achieved by means a structure in which the

> via hole is first lined with a layer of silicon nitride prior to adding the diffusion barrier and copper. This allows use of a barrier layer that is thinner than normal (since the silicon nitride liner is an effective diffusion barrier) so that more copper may be included in the via hole, resulting in an improved conductance of the via.

Despite the presence of a silicon nitride layer, Lin still requires the use of a barrier layer of 100 to 2000 Angstroms of Ta or TaN. By contrast a much thinner 30 to 500 Angstrom (~25%) layer is used in the instant invention.

The Examiner observes:

> 7. Further, Lin teaches using etchant gases containing CHF3 and CF4 mixed with oxygen. It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the well known teachings of using fluorocarbon and oxygen etch chemistry, as exemplified by Lin, to etch the materials of the first and second insulator, the etch stop, and the protective layer, in order to etch these materials quickly and under control, while also producing volatile exhaust gases that helps keep the wafer and chamber cleaner from contaminants. In addition, it is well known in the art to employ inert carrier gasses, such as Ar and Nitrogen. It would have been obvious to one of ordinary skill in the art at the time of the invention to use Ar and nitrogen to control the etchant concentration in the chamber, thereby better controlling the etch rate of the material being etched, thereby reducing the chances of over-etching the material.

The Applicants respond by noting that in Lin's specification, CHF_3 and CF_4 mixed with oxygen is applied to items 21, 71, 72 and 92, which are respectively found at column 1, line 32, column 4, line 4, column 3, line 38 and column 4, line 4 defined respectively as silicon oxide, silicon nitride, silicon oxide and silicon nitride. Silicon oxide and silicon nitride are not low-K dielectrics. Furthermore, Lin's only use of the word "low" is to modify the words "resistance", "selectivity" and "pressure". Therefore there are no low-K dielectrics in Lin. Lin does not teach low-K dielectrics. Lin does not teach etching of low-K dielectrics. CHF_3 (or CF_4) plus oxygen is used to etch silicon oxide and silicon nitride.

Furthermore, C_2F_6, C_4F_8, Ar, N_2 and O_2 are the components of a recipe the

Applicants use to etch low-K dielectrics. It is a recipe that is not of Lin and most likely would be of no use to Lin.

> 13. Applicant asserts that Lin teaches a barrier layer 100 to 2000 angstroms, while the claimed invention only claims 30-500 angstroms. The ranges overlap and therefore the claimed invention infringes on Lin.
>
> 14. Applicant attacks the Lin reference asserting that Lin does not teach the etching of low-K dielectrics, but rather silicon oxide and nitride. Applicant further asserts that the claimed recipe would be of no use to Lin. Applicant's attention is directed to applicant's claim 19 and 24, which teach applicant's claimed recipe is used to etch an etch stop layer, which is claimed to consist of silicon nitride. In response to applicant's arguments against the references individually, one cannot show non obviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986).

Respectfully, the Applicants do not "attack" this reference individually. The Applicants quite clearly state that Lin does not provide the same gas components and recipe for the service needed, namely etching low-k materials. This is not an "attack" but a statement of fact of where Lin does not fit into the combination of references of which the Examiner opines.

Furthermore, Since Lin is not etching low-k dielectrics, he would not be interested in recipes that etch low-k dielectrics. Similarly, since the Applicants are etching low-k dielectrics, they are not interested in recipes that etch SiN_2.

The fact that the instant invention has an etch-stop layer of SiN_2 or other material to etch, as the Examiner has noticed, is not the major issue, and diverts the attention from that of etching low-k materials.

Action Items 8 & 15

35 USC § 103(a) Claims Rejection

Reconsideration of the rejection of Claims 2, 6, 17 and 21 under 35 U.S.C. 103(a) as being unpat ntable over Zhou et al. as applied to claims 1, 3-5,

7-10, 12-16, 18-20, 22, 25-26, 28 and 30 above, and further in view of Eissa et al. (US 2002/0127876) is requested based on the following arguments:

Eissa et al. has a file date of May 10, 2002. The instant application has a file date of May 24, 2001 which predates the reference by almost one year.

The Examiner observes:

> 8. Zhou appears not to specify the k value of the low-k dielectric used in the first and/or the second dielectric. Eissa teaches the use of a low-k dielectric in a copper dual damascene interconnect structure having a k value between 2.0 and 3.0, page 1, par. [0010]. It would have been obvious to one of ordinary skill in the art at the time of the invention to select a low-k dielectric having a k-value between 2.0 and 3.0 in an interconnect structure having copper, in order to reduce the parasitic capacitance of the interconnect thereby reducing the RC constant and increasing the speed and performance of the devices.

The Applicants reply by asserting that they are using a low-K dielectric with the low resistance conductor copper for the obvious reason of achieving an increase in speed and performance due to the well known approach of reducing the RC time constant. It is what almost everyone practicing the art is doing. Eissa et al. does not teach anything new in this regard. The Applicants, as well as the current and prior art practitioners, are using commercial low-K dielectric products like FLARE, SiLK, etc. which are advertised to have low dielectric constant. Eissa et al. have merely discovered another way to control the generation of defects of poisoning copper damascene in low-K dielectrics, which the Applicants do not employ.

> 15. Finally, applicant asserts that Eissa teaches the use of commercial low-k dielectric products, which are well known in the art, thus not teaching anything new. The cited art is used in the rejection to merely assert that the use of a low-k dielectric with a value between 2 and 3, is known and would be obvious. Applicant's arguments seem to be confirming the examiner's assertion.

The Applicants reply that Claims 2, 6, 17 and 21 are d pend nt on their

respective independent claims 1 and 13.

CONCLUSION

It is respectfully suggested that these various references cannot be combined without reference to applicants' own invention. It is believed that independent claims 1 and 13, and hence claims dependent from claim 1, and claims dependent from claim 13, as amended, are allowable, and we therefore request respectfully that Examiner Berezy reconsider these rejections in view of these arguments and the amendments and allow claims 1 through 30

We have reviewed the related art references made of record and agree with the Examiner that none of these suggest the present claimed invention.

In light of the above arguments, it is suggested that the specification now adequately describes the invention and that the Claims now clearly distinguish the invention from the prior art. All claims are therefore believed to be in condition for allowance.

Allowance of all claims is therefore respectfully requested.

It is request that should Examiner Berenzy not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B Ackerman, Reg. No. 37,761

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1. (CURRENTLY AMENDED) A method to solve via poisoning for insulative porous low-k materials comprising the steps of:

providing a substrate having a first and a second insulative layers separated from each other by an intervening etch-stop layer formed therein said substrate;

forming a hole opening in said first and second insulative layers, including said intervening etch-stop layer;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a trench opening over said hole opening to form a dual damascene structure;

forming a barrier layer on the vertical walls of said trench opening and on said low-k protection layer on the vertical walls of said hole opening;

forming a metal layer over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP), to complete the forming of said

dual damascene structure.

8. (CURRENTLY AMENDED) The method of claim 1, wherein ,said low-k protection layer comprises SiO2, SiN, SiC [and] or SiNC.

13. (CURRENTLY AMENDED) A method to solve via poisoning for insulative porous low-k materials in a dual damascene structure comprising the steps of:

providing a substrate having a passivation layer formed over a first metal layer formed on said substrate;

forming a first insulative layer over said substrate;

forming an etch-stop layer over said first insulative layer;

forming a second insulative layer over said etch-stop layer;

forming a first photoresist layer over said second insulative layer and patterning said photoresist to form a first photoresist mask having a hole pattern;

etching said first and second insulative layers, including said etch-stop layer through said hole pattern to form a hole reaching said passivation layer;

removing said first photoresist mask;

forming a low-k protection layer over said substrate, including in said hole opening;

forming a second photoresist layer over said substrate, including said hole opening and patterning said second photoresist to form a second photoresist mask having a trench pattern; .

etching said second insulative layer through said trench pattern in said second photoresist mask to form a trench in said second insulative layer, thus completing the forming of said dual damascene structure in said substrate;

removing said second photoresist mask;

removing said low-k protection layer from over said substrate and from the bottom of said hole opening and thereby exposing underlying said passivation layer while leaving said low-k protection layer on the vertical sides of said hole opening;

removing said passivation layer from said bottom of said hole opening, thereby exposing underlying said first metal layer;

forming a barrier layer over said substrate, including in said dual damascene structure, wherein said barrier layer conforms to said low-k protective layer in said hole opening and conforms to said trench in said second insulative layer;

depositing a second metal over said barrier layer in said dual damascene structure; and

performing chemical mechanical polishing (CMP) to complete the forming of said dual damascene structure.

25. (CURRENTLY AMENDED) The method of claim 13, wherein said low-k protection layer comprises SiO_2, SiN, SiCN [and] or SiC.